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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/801,130 | 03/16/2004 | Georg Eggers | 543822005100 | 9233 |

25227 7590 04/20/2007

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| EXAMINER | |
|---|---|
| RAHMAN, FAHMIDA | |
| **ART UNIT** | **PAPER NUMBER** |
| 2116 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 04/20/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/801,130 | EGGERS ET AL. | |
| | Examiner | Art Unit | |
| | Fahmida Rahman | 2116 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This final action is in response to communications filed on 1/22/2007.

2. Claims 1-16 have been amended, no new claims have been added, no claims have been cancelled. Thus, claims 1-16 are pending.

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 11, 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Noble et al (US Patent 5914870).

For claim 1, Noble et al teach the following limitations:

A system comprising:

A synchronizer signal generator device (212), to be connected to an electronic system (218, 222, 19 and 22), the synchronizer signal generator device to emit a synchronizer signal (signal on line 246) of a particular frequency (246 has a particular frequency since it is a sinusoid as mentioned in lines 48 of column 6), which is transferred to at least one receiving device (218) of the electronic system; at least one additional device (214), of which an impedance is chosen (L is chosen as 68 micro henry mentioned in line 13 of column 5) such that a

resonance-oscillatory circuit is created (209 forms a resonant circuit with that inductance mentioned in lines 15-20 of column 5), for the synchronizer signal generator device (resonance-oscillatory circuit is created for 212) having resonance frequency (lines 10-25 of column 5) essentially coincides with the frequency of the synchronizer signal (when resonance is formed, output of AND gate strikes 209 at its resonance frequency. Thus, signal on 246 has resonance frequency) and a clock generator device (202, 201) to generate a clock signal having a frequency (202 generates clock as shown in Fig 2), wherein the clock generator device is controlled by the synchronizer signal (synchronizer signal on 246 controls 232 that in turn controls 238 and 201. Therefore 201 is controlled by signal on 246) and frequency of the synchronizer signal is greater than the frequency of the clock signal (line 64 of column 4 through line 26 of column 5 mentions that input clock signal is 345.6 KHZ and resonant frequency 360.3 KHZ. When the circuit is in resonant frequency, synchronizer signal is also in resonance frequency. Therefore, synchronizer signal frequency, at resonance state of the circuit, is greater than clock frequency).

For claim 2, line 47 of column 6 mentions that signal is sinusoid.

For claim 3, 242 is the driver.

For claim 11, the receiving device 218 is semiconductor diode.

For claim 16, Noble et al teach the following limitations:

A process for generating a synchronizer, comprising: emitting a synchronizer signal (signal on line 246) from a synchronizer signal generator device (212) to at least one receiving device (218) of an electronic system (218, 222, 19 and 22); and providing the at least one additional device (214), for which an impedance has been selected (L is chosen as 68 micro henry mentioned in line 13 of column 5) such that, a resonance-oscillatory circuit is created (209 forms a resonant circuit with that inductance mentioned in lines 15-20 of column 5) for the synchronizer signal generator device (resonance-oscillatory circuit is created for 212), the resonance-oscillatory circuit having a resonance frequency which essentially coincides with a frequency of the synchronizer signal (when resonance is formed, output of AND gate strikes 209 at its resonance frequency. Thus, signal on 246 has resonance frequency); and generating a clock signal (output of 202) at a clock generator device (201 and 202), wherein the clock generator device is controlled by the synchronizer signal (synchronizer signal on 246 controls 232 that in turn controls 238 and 201. Therefore 201 is controlled by signal on 246), and the frequency of the synchronizer signal is greater than a frequency of the clock signal (line 64 of column 4 through line 26 of column 5 mentions that input clock signal is 345.6 KHZ and resonant frequency 360.3 KHZ. When the circuit is in resonant frequency, synchronizer signal is also in resonance frequency. Therefore, synchronizer signal frequency, at resonance state of the circuit, is greater than clock frequency).

**Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al (US Patent 5914870),

For claim 4, the embodiment of Fig 2 does not show that the output of 242 is rectangular. However, the alternate embodiment in Fig 6 shows 616 as PWM generator. It is well known in the art that PWM typically produces rectangular pulse. One ordinary skill would be motivated to use PWM generator to produce rectangular pulse for its availability to one ordinary skill.

For claim 5, 611 is the filter.

For claim 6, Noble does not teach the inductive component. However, the filter 611 is a low pass filter and can be designed with inductive component, for example, a butterworth filter. One ordinary skill would prefer the butterworth filter with inductive component for its flat response.

For claim 7, 613 is capacitive.

For claim 8, typically the filter 611 is designed during manufacture.

5. Claims 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al (US Patent 5914870), in view of Harvey (US Patent 5734285).

For claims 12 and 13, Noble et al do not teach that the synchronization signal is for coordination of data transfer or, an additional signal is generated from the synchronization signal to coordinate data transfer.

Harvey teaches that the synchronizer signal generating device (50) generates further signal (FB) under control of the synchronizer signal (CKR, FB is under control of CKR, since the purpose of FB is to control 58 to produce tuned CKR), which is to be used for chronological co-ordination of processing of data (CKR is clock, which is used for chronological co-ordination of data).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Noble and Harvey. One ordinary skill would be motivated to have a signal for coordination of data as coordination is a desired feature in electronic circuit.

For claims 14 and 15, neither Noble nor Harvey teaches that further signal has lower frequency or PLL/DLL used for generating further signal.

Examiner takes an official notice that using PLL/DLL to produce the secondary clock to latch data is also well known in the art. An ordinary skill in the art would be motivated to use PLL/DLL to produce a secondary clock, which has a lower frequency than primary clock, to latch the data signal since using a secondary clock to latch user entered data signal to the circuit of Noble et al.

6. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al (US Patent 5914870), in view of Cruz et al (US Patent 6396316).

For claim 9, Noble et al do not teach the adjustment of inductive or capacitive component. Cruz et al teach the adjustment of capacitive component (abstract).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Noble et al and Cruz et al. One ordinary skill in the art would have been motivated to adjust the capacitance to permit the resonant frequency to be adjusted.

For claim 10, neither Noble et al nor Cruz et al teach that the capacitive diode. Examiner takes an official notice that capacitive diode is well known in the art. One ordinary skill in the art would be motivated to use the capacitive diode for its advantageous use in voltage controlled oscillator.

**Response to Arguments**

Applicant's arguments filed on 1/22/2007 have been fully considered but they are not persuasive.

Applicant argues that Noble does not teach or suggest forming a resonance-oscillatory circuit with a synchronizer signal such that a synchronizer signal to control a clock signal such that the frequency of the synchronizer signal is greater than the frequency of the clock signal.

Examiner disagrees. Noble teaches at least one additional device (214), of which an impedance is chosen (L is chosen as 68 micro henry mentioned in line 13 of column 5) such that a resonance-oscillatory circuit is created (209 forms a resonant circuit with that inductance mentioned in lines 15-20 of column 5), for the synchronizer signal generator device (resonance-oscillatory circuit is created for 212) having resonance frequency (lines 10-25 of column 5) essentially coincides with the frequency of the synchronizer signal (when resonance is formed, output of AND gate strikes 209 at its resonance frequency. Thus, signal on 246 has resonance frequency) and a clock generator device (202, 201) to generate a clock signal having a frequency (202 generates clock as shown in Fig 2), wherein the clock generator device is controlled by the synchronizer signal (synchronizer signal on 246 controls 232 that in turn controls 238 and 201. Therefore 201 is controlled by signal on 246) and frequency of the synchronizer signal is greater than the frequency of the clock signal (line 64 of column 4

through line 26 of column 5 mentions that input clock signal is 345.6 KHZ and resonant frequency 360.3 KHZ. When the circuit is in resonant frequency, synchronizer signal is also in resonance frequency. Therefore, synchronizer signal frequency, at resonance state of the circuit, is greater than clock frequency).

Official notices taken on action dated on 9/20/2006 on various subjects have not been argued by the applicant. Therefore, they are considered admitted prior art.

**Conclusion**

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action. Any inquiry concerning this communication or earlier communications from the examiner should be directed

to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Fahmida Rahman
Examiner
Art Unit 2116

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THUAN N. DU
PRIMARY EXAMINER